

Intel H61 MATX Schematic

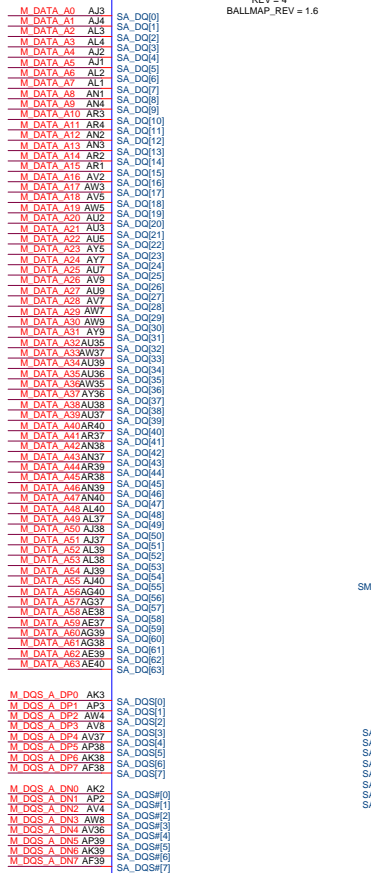
H61GV80B_0529 vga加电阻

在H61GV80a基础上修改

Version: 1.0

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Title			
Cover Sheet			
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M_DQS_A_DP[0..7] 8
M_DQS_A_DN[0..7] 8

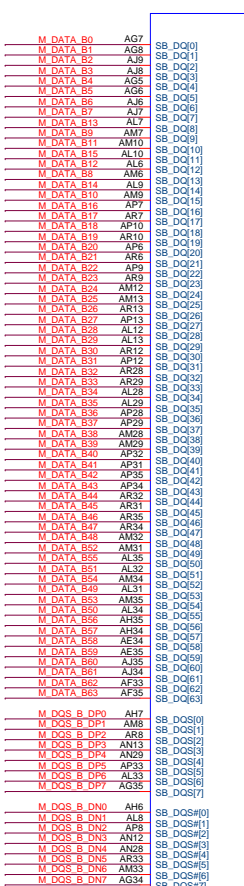


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SKT_H2

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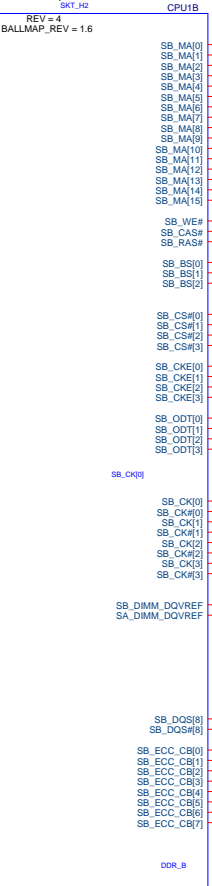
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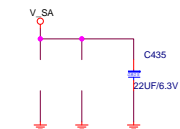
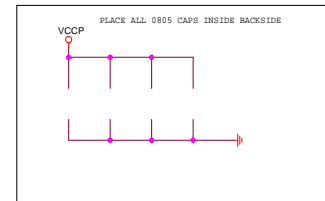
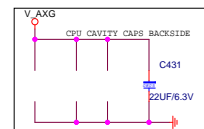
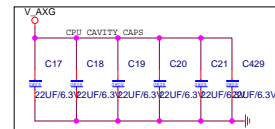
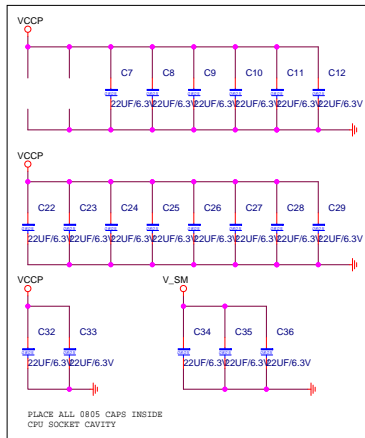
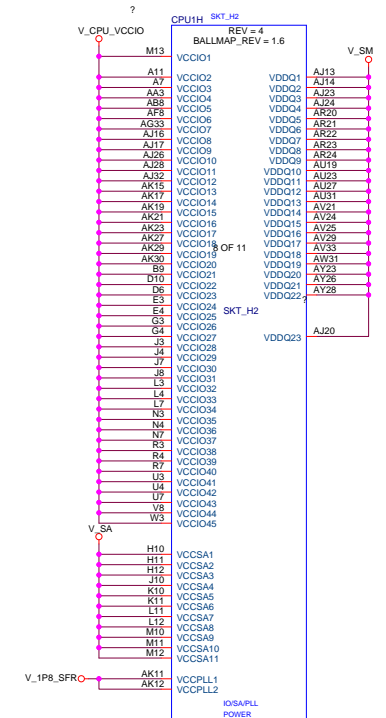
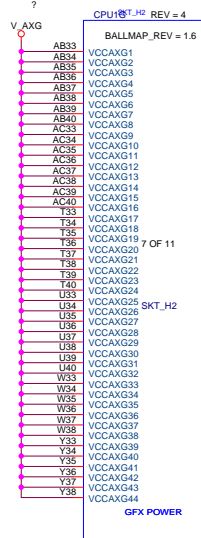
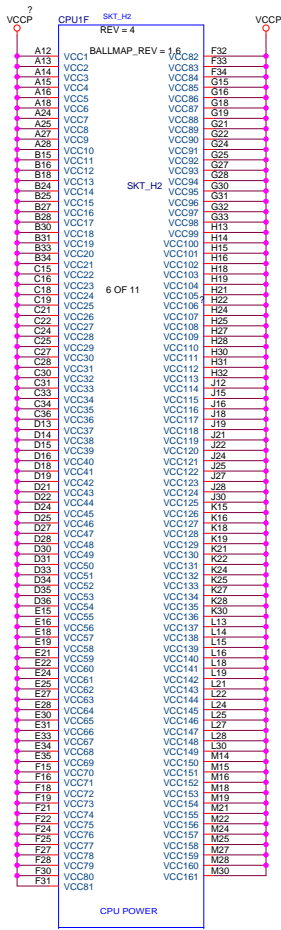


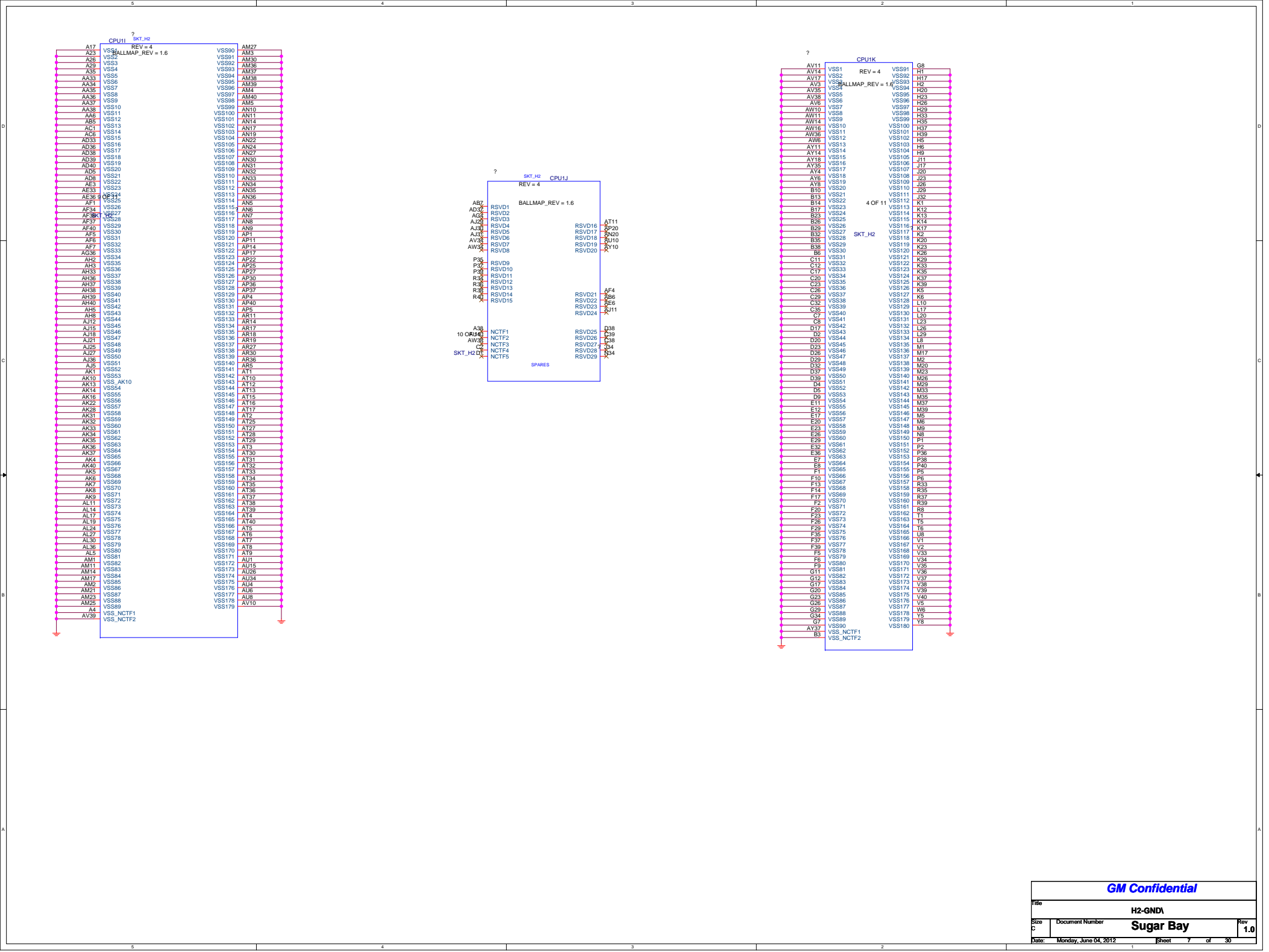
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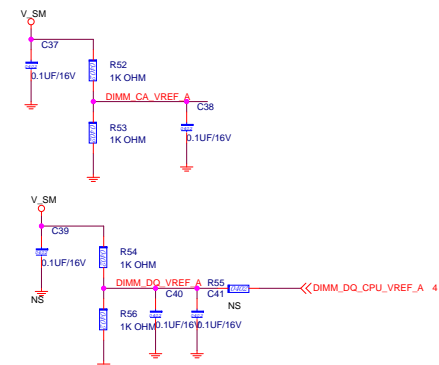
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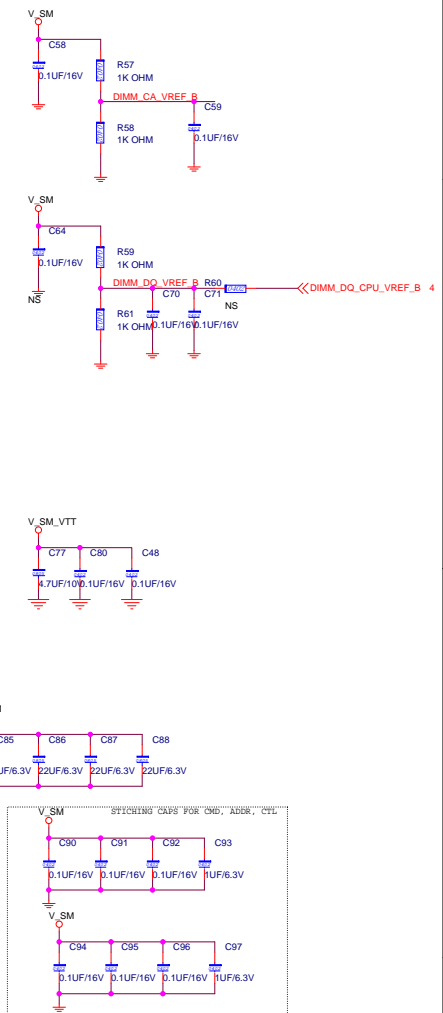
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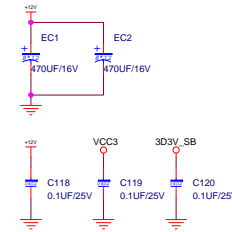
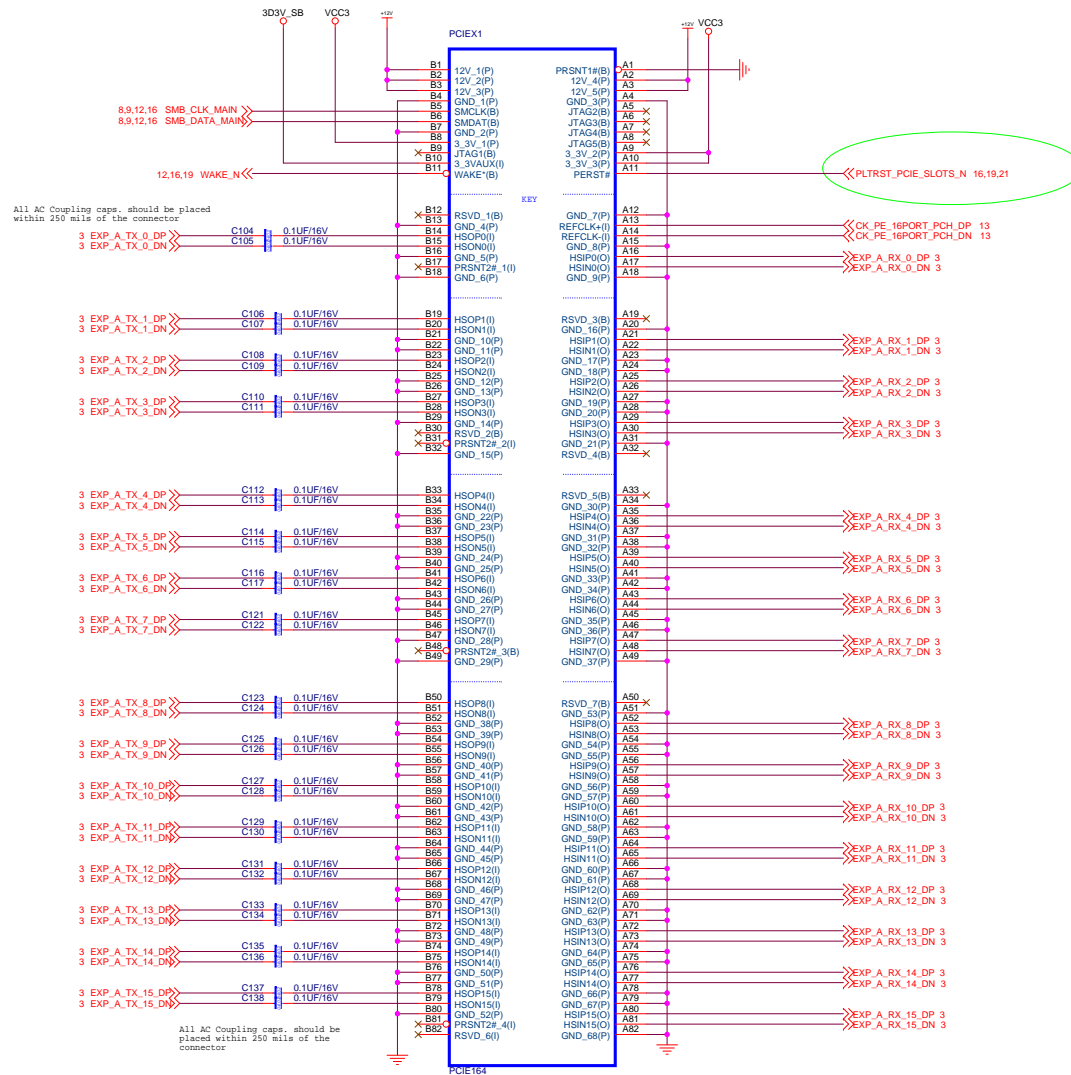


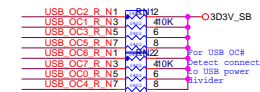
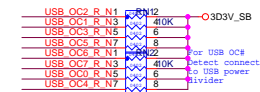
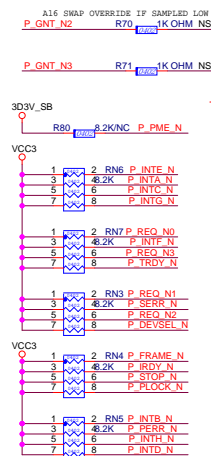




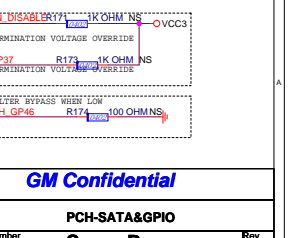
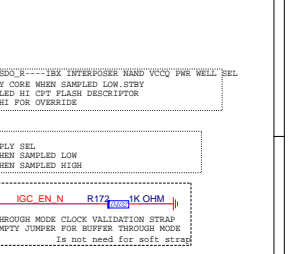
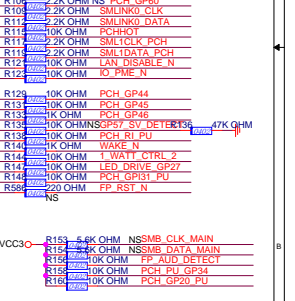
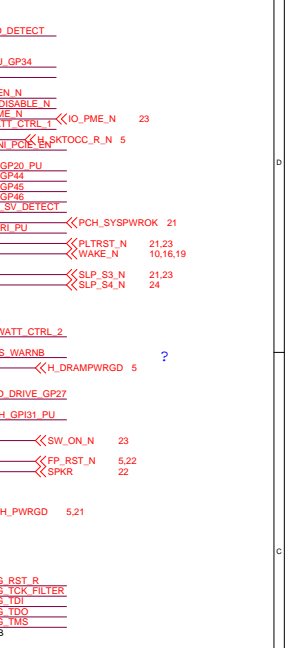
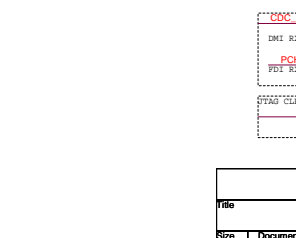
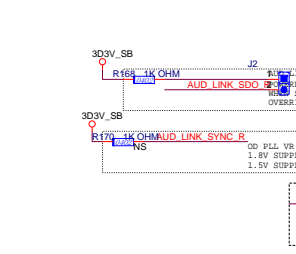
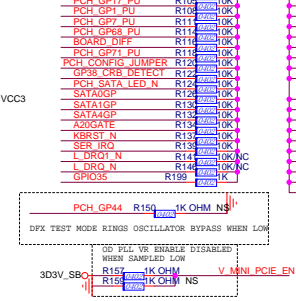
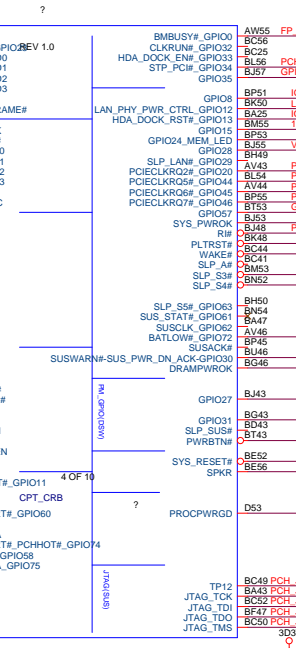
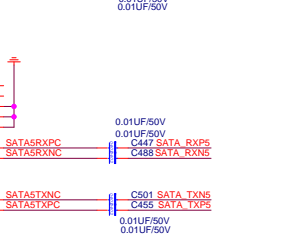
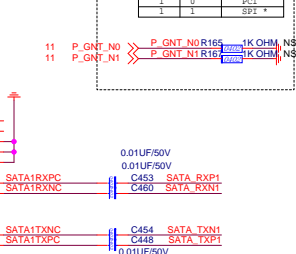
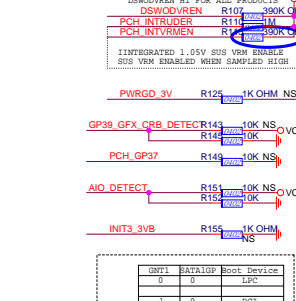
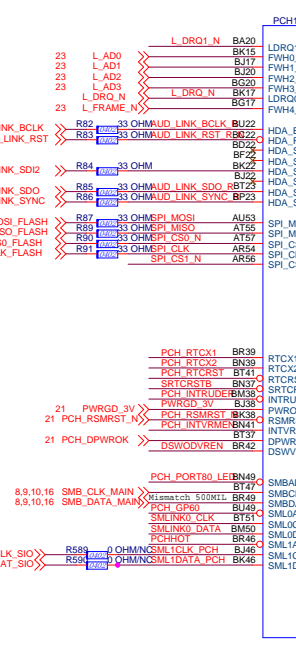
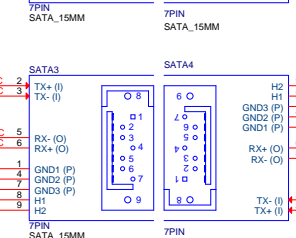
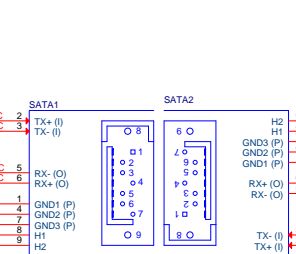
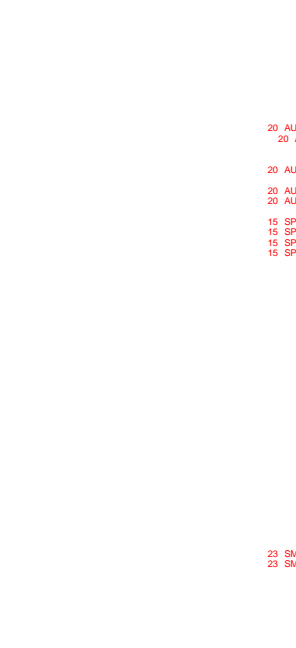
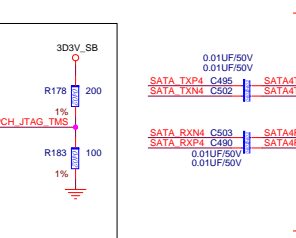
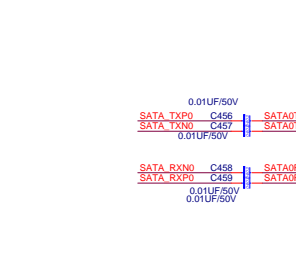
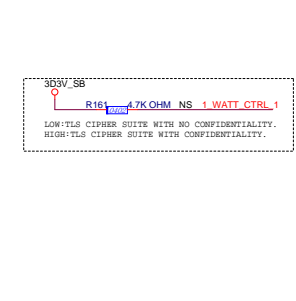
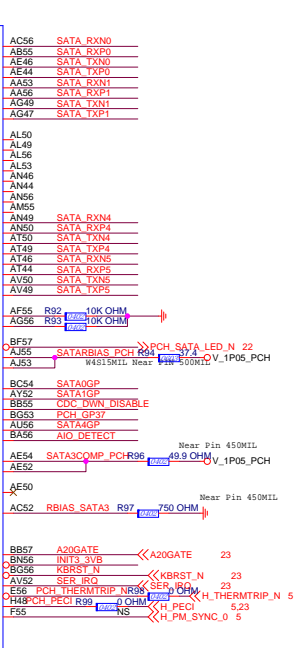
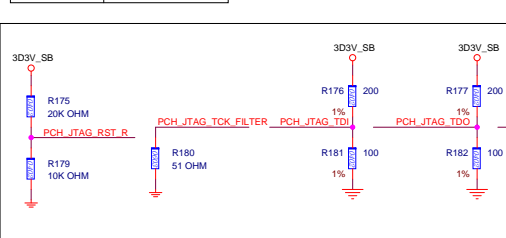
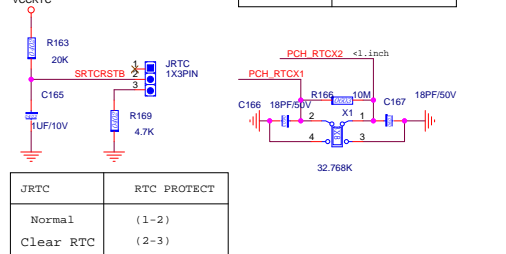
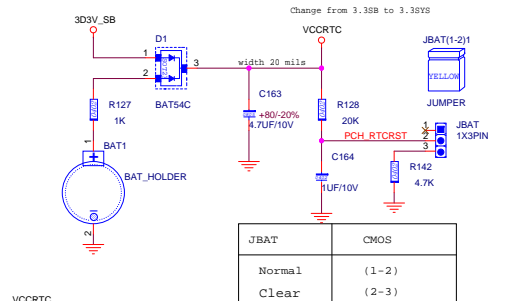
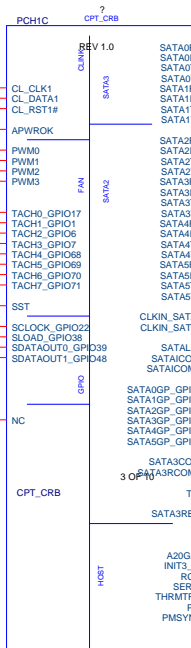


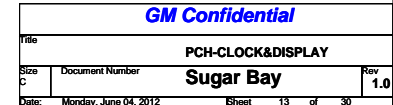


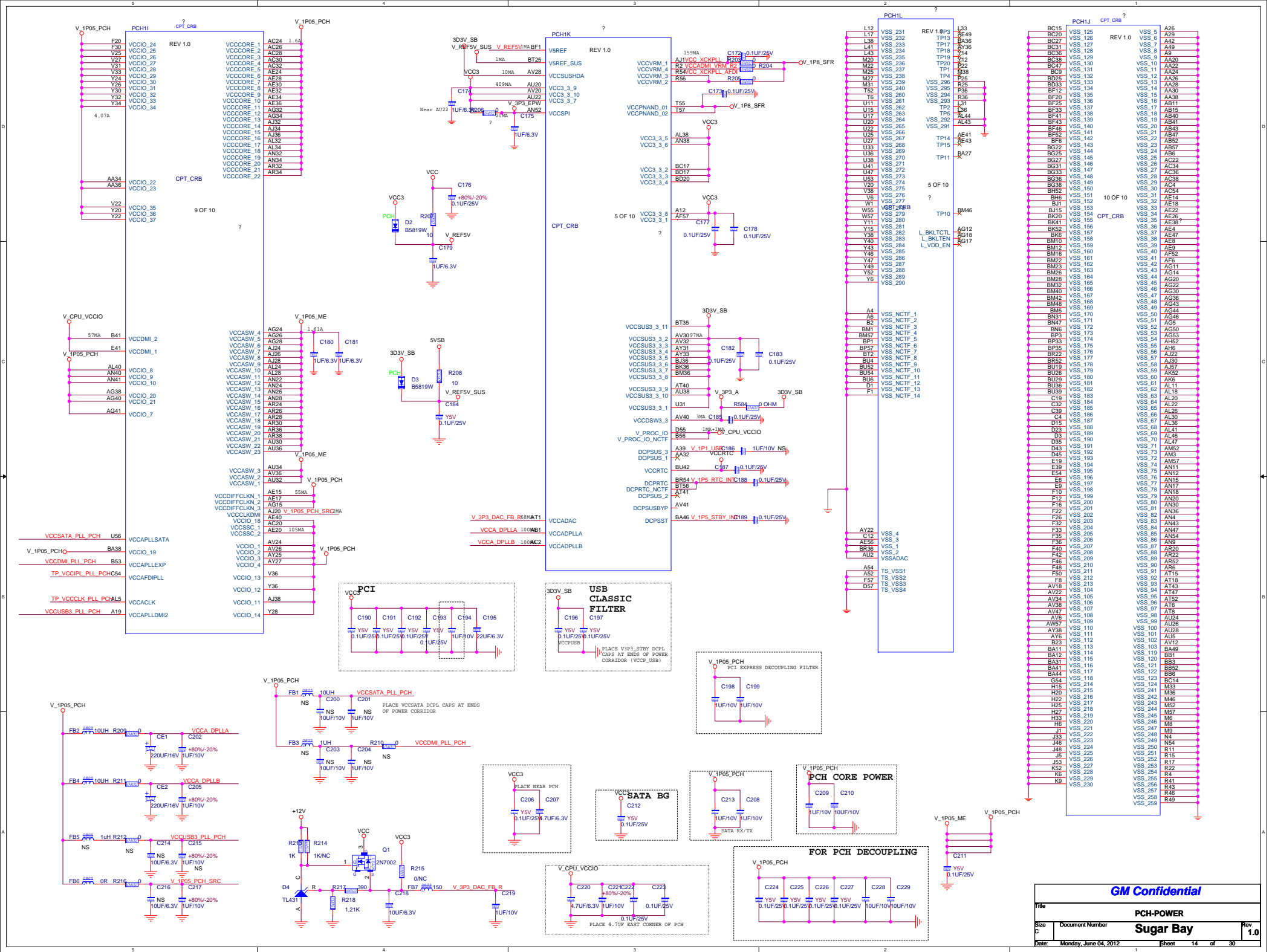




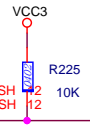
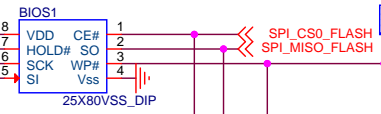
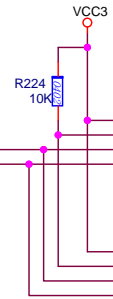
21 PWRGD_3V



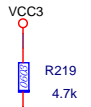




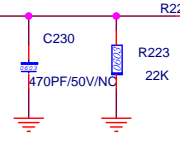
12 SPI_CLK_FLASH
12 SPI_MOSI_FLASH



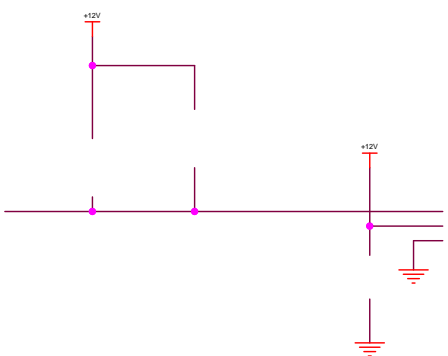
23 FAN_CTL1



23 FAN_TAC1



23 FAN_TAC3



System FAN 2

100

27k

0

23

+12V

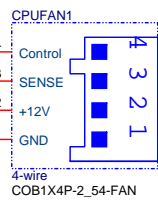


4.7k

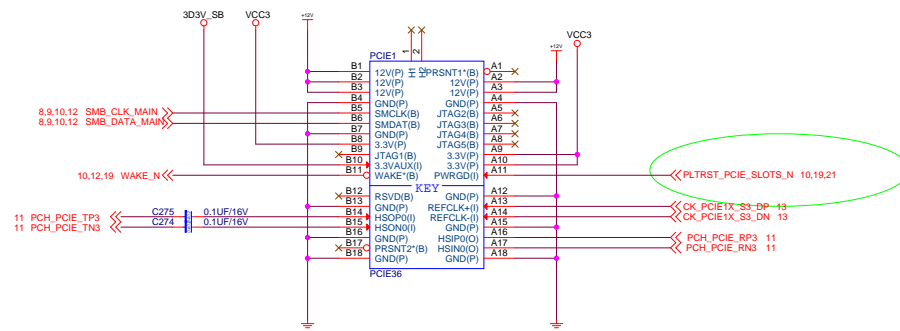
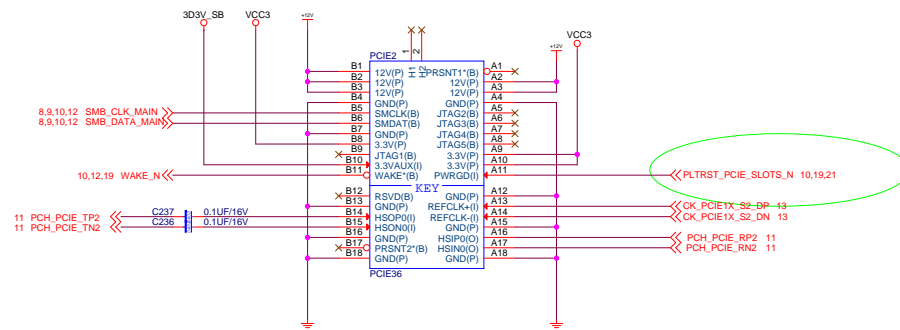
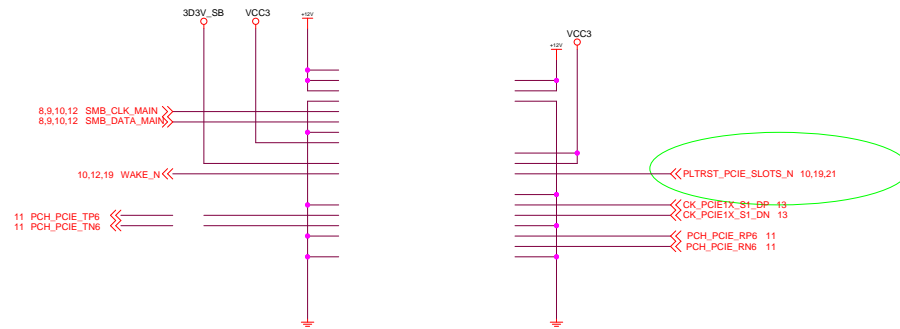
+12V



0.1UF/50V

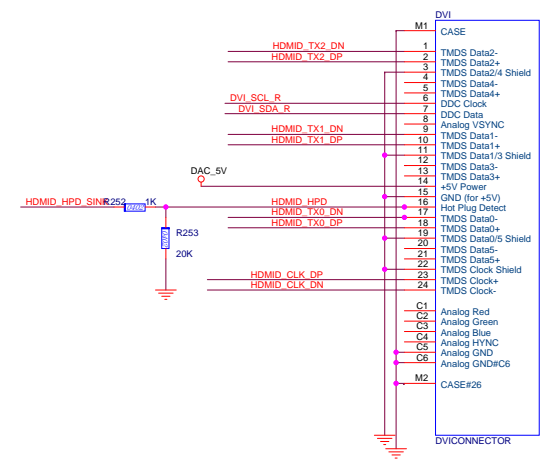
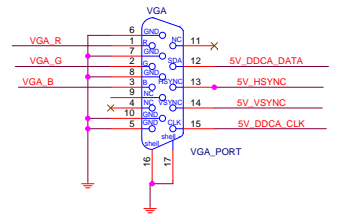
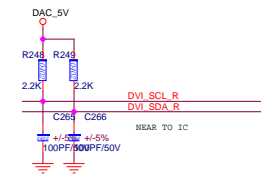
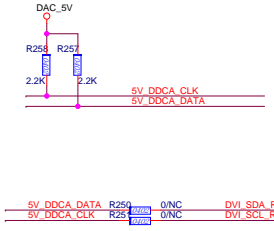
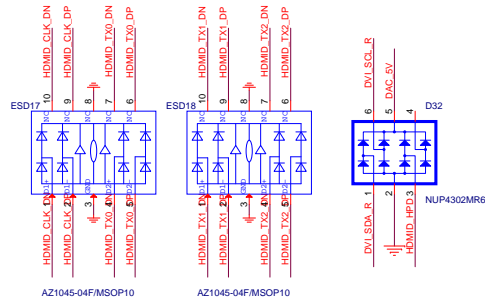
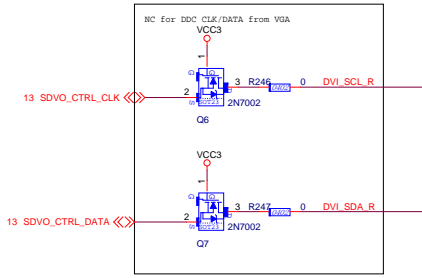
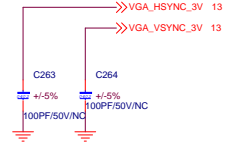
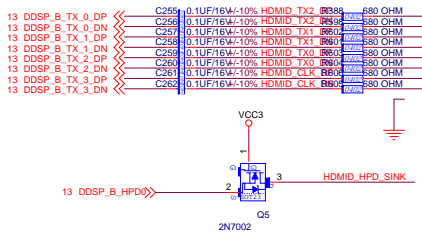
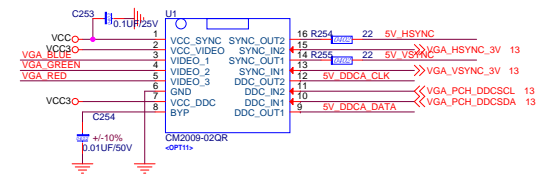
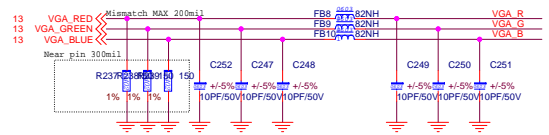
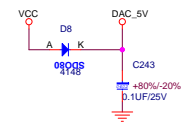


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SPI&DEBUG PORT			
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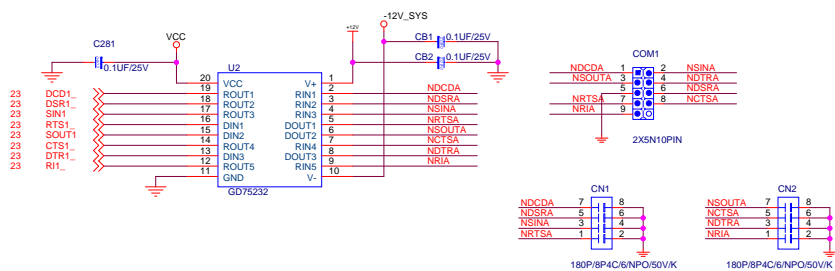
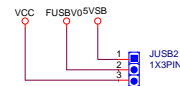
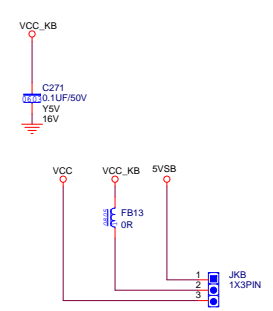


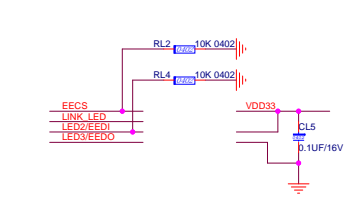
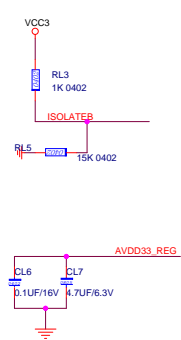
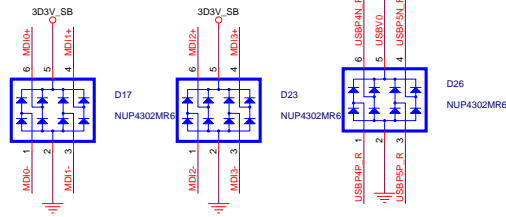
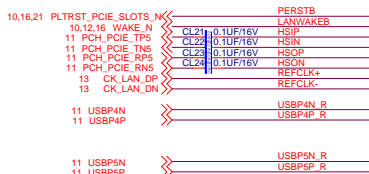
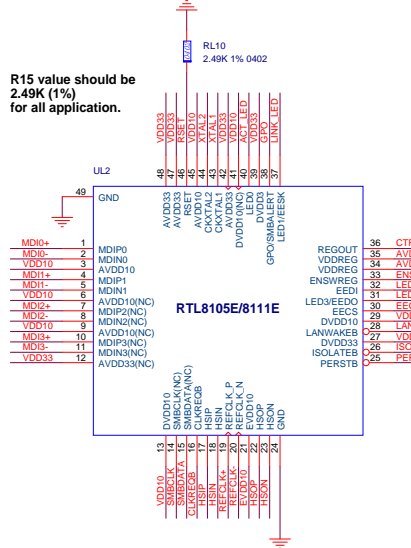
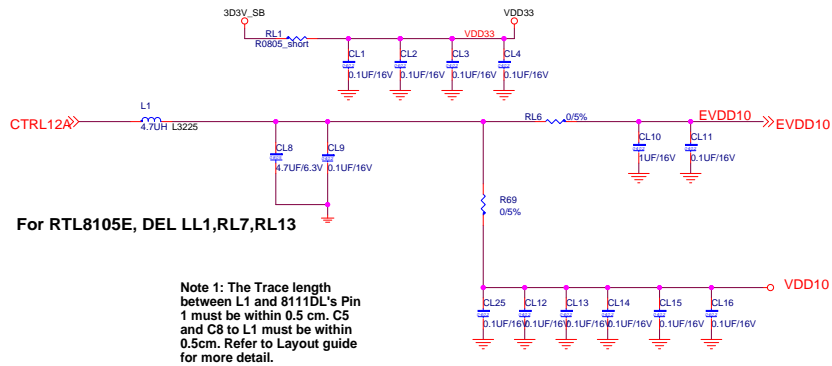
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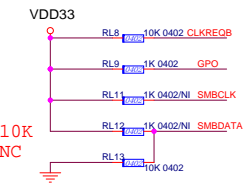
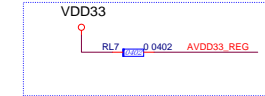


Design Note: For DVI-I Support Please Use Port B See MOW WW07 For Detail.



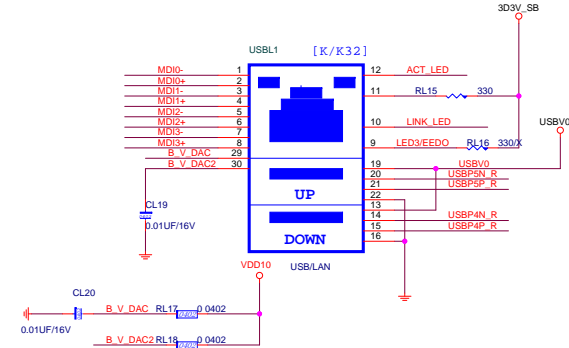


For RTL8111E, use this block



**8111E RL13 10K
8105E RL13 NC**

For RTL8105E, Del RL14, Add RL19



[illegible][illegible][illegible]

VCC3

RA26 10K

CA14 0.01uF 16V Y5V

CA17 100P 50V NPO

J13

SPDIF 1 2 3 3*1 PIN

CA15 0.01uF 6V Y5V

RA28 100

CA22 100P 50V NPO

RA30 100P 50V NPO

SPD OUT R

VREFO

MIC1-VREFO-R

RA18 10K/5%

RA19 10K/5%/X

RA20 10K/5%

MIC IN

MIC1 IN_R

MIC1 L

CA6 1uF

RA23 75/5%

MIC1 IN_L

LINE IN

LINE1_R

CA9 1uF

RA29 75/5%

L IN_R

LINE1_L

CA10 1uF

RA31 75/5%

L IN_L

LINE OUT

The diagram illustrates the AC97 Front Audio section of the PCB. It includes the following components and connections:

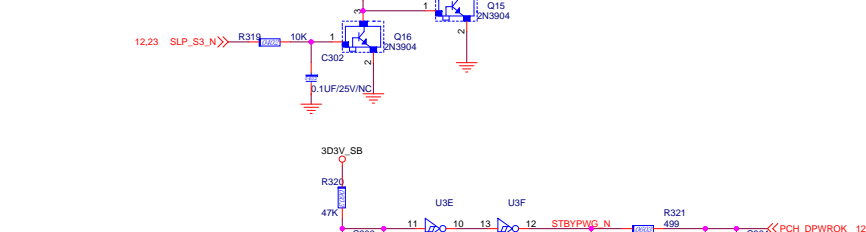
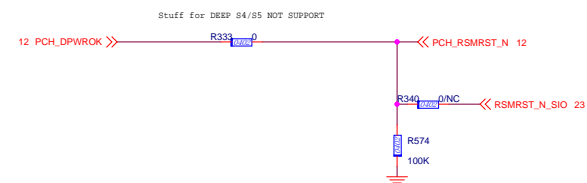
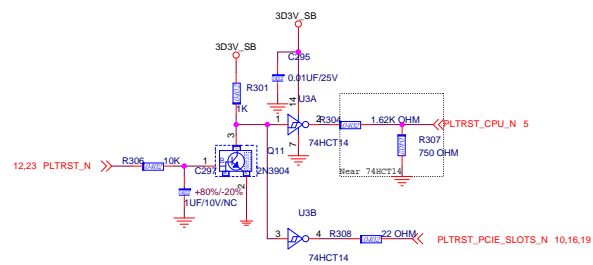
- Microphone Inputs:**
 - MIC2:** MIC2_L and MIC2_R inputs connected to CA20 and CA21 (100nF capacitors) and RA43, RA44 resistors.
 - MIC1:** MIC1_IN_L and MIC1_IN_R inputs connected to RA41, RA42 resistors.
- Line Inputs:**
 - LINE2:** LINE2_VREF and LINE2_IN connected to RA49, RA51 resistors.
 - LINE1:** LINE1_IN_L and LINE1_IN_R inputs connected to RA13, RA14 resistors.
- Output Drivers:**
 - SR4, SR5, SR6, SR7:** Output drivers for the audio signals, connected to GND_AUD.
 - RA16, RA17:** Resistors for the output drivers.
- Connectors:**
 - CFPA HEADER2X5:** A 2x5 pin header for the microphone inputs.
 - 13PIN CON13P-PHONEX3:** A 13-pin connector for the front audio output.
- Labels:**
 - CD IN:** Label for the CD input section.
 - AC97 FRONT AUDIO:** Label for the AC97 front audio section.

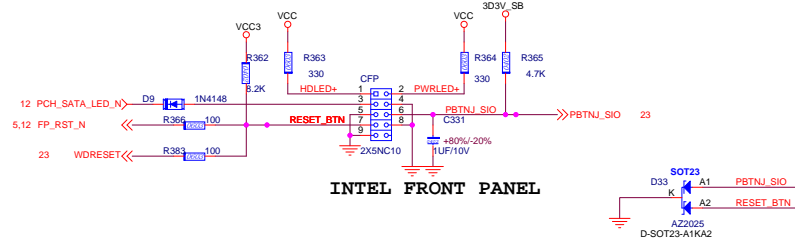
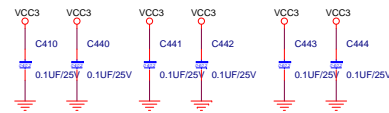
The diagram illustrates the AC97 Front Audio section of the PCB. It includes the following components and connections:

- Microphone Inputs:**
 - MIC2:** MIC2_L and MIC2_R inputs connected to CA20 and CA21 (100nF capacitors) and RA43, RA44 resistors.
 - MIC1:** MIC1_IN_L and MIC1_IN_R inputs connected to RA41, RA42 resistors.
- Line Inputs:**
 - LINE2:** LINE2_VREF and LINE2_IN connected to RA49, RA51 resistors.
 - LINE1:** LINE1_IN_L and LINE1_IN_R inputs connected to RA13, RA14 resistors.
- Output Drivers:**
 - SR4, SR5, SR6, SR7:** Output drivers for the audio signals, connected to GND_AUD.
- Connectors:**
 - CD IN:** A connector for the CD input, with pins for CDL, CDG, and CDR.
 - AC97 FRONT AUDIO:** A 13-pin connector for the AC97 front audio interface.
- Other Components:**
 - RA41, RA42:** Resistors for MIC1_IN_L and MIC1_IN_R.
 - RA43, RA44:** Resistors for MIC2_L and MIC2_R.
 - RA49, RA51:** Resistors for LINE2_VREF and LINE2_IN.
 - RA13, RA14:** Resistors for LINE1_IN_L and LINE1_IN_R.
 - CA20, CA21:** 100nF capacitors for MIC2_L and MIC2_R.
 - CA23, CA25:** 100nF capacitors for SUR_BACK_OR and SUR_BACK_OL.
 - CA18, CA19:** 100pF capacitors for the output drivers.

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ALC888-VC/892			
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Symbol	value	Description
JP3	Flashseg1_EN	1 Disabled
Pin 124		0 Flash I/F Address Segment 1 is enabled
JP4	K8PWR_EN	1 K8 power sequence function is disabled
Pin 126		0 K8 power sequence function is enabled
		11 The default value of EC Index 15v/16h/17h is 80h
JP3 & JP5	FAN_CTL_SEL	10 The default value of EC Index 15v/16h/17h is FFF(Fan off)
Pin 124 & Pin 126		01 The default value of EC Index 15v/16h/17h is 00h(Fan full speed)
		00 The default value of EC Index 15v/16h/17h is 40h

```

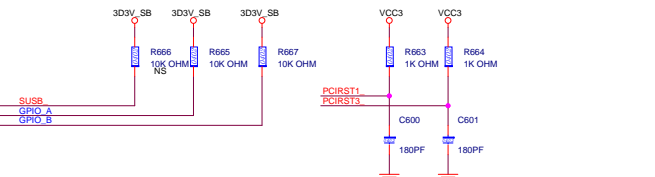
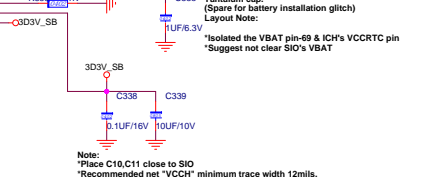
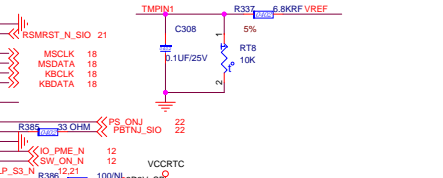
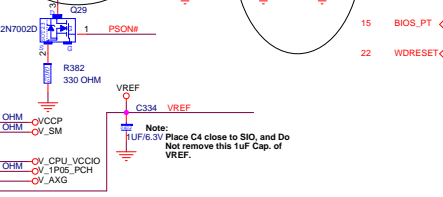
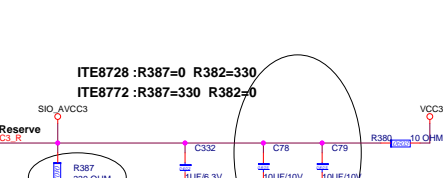
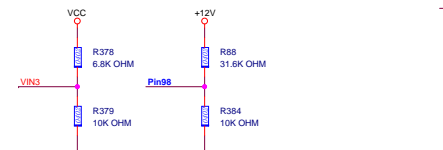
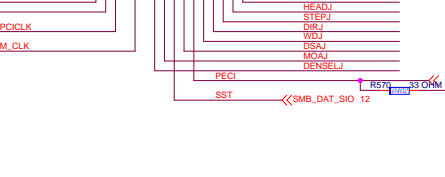
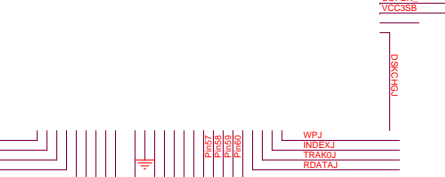
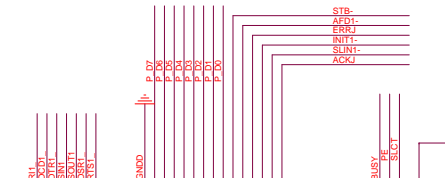
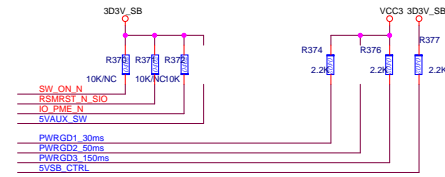
If without use these pins, Please
Don't let it floating
1.Pin 95:VIN3/ATXPG
2.Pin 71:SUSB#
3.Pin 3:PCIRSTIN#
4.Power On Strapping Options pin
5.Pin80~83 KCLK/KDAT/MCLK/MDAT

```

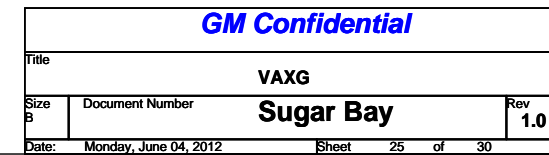
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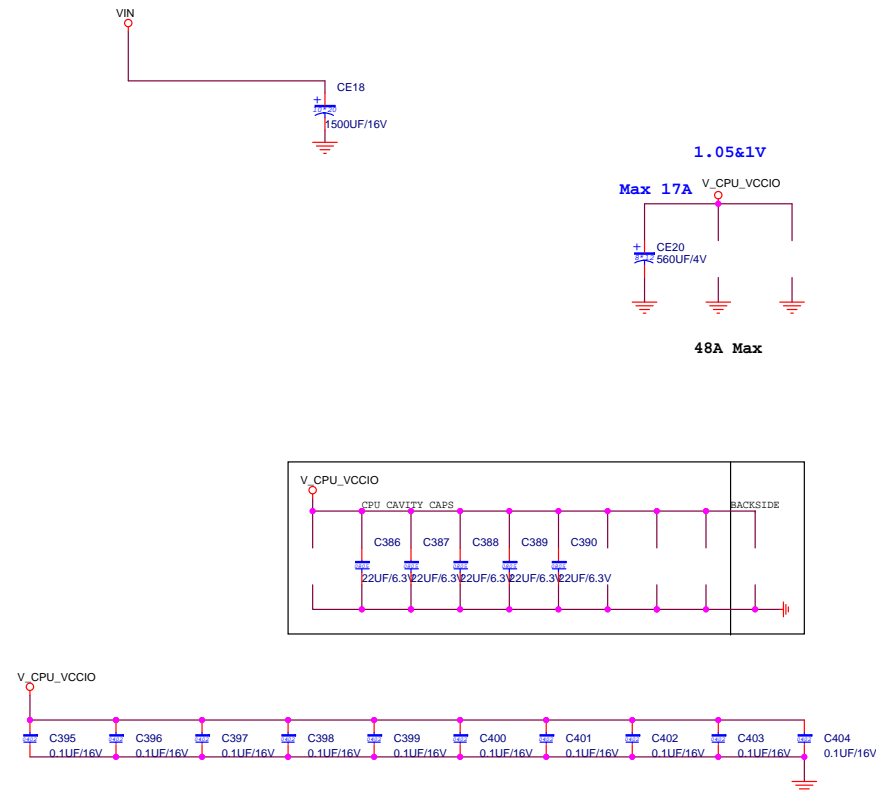
18 SIN1
18 SOUT1
18 DSR1_
18 RTS1_
18 RI1_
18 DCD1_
18 DTR1_
18 CTS1_

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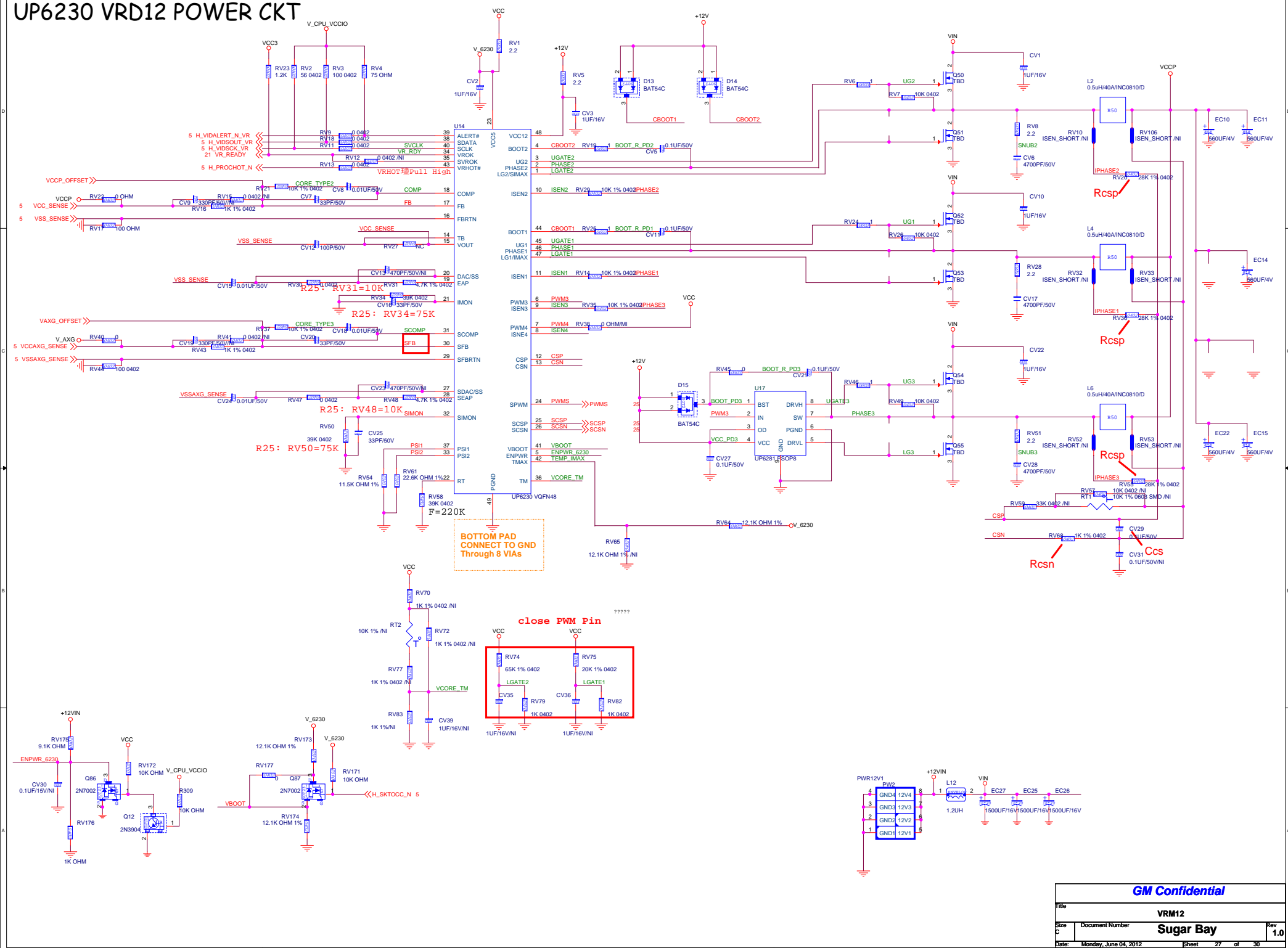
[illegible]

P12页 KBRST A20GATE 上拉电阻R134 R137改为1K





UP6230 VRD12 POWER CKT



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